FIG. 1A

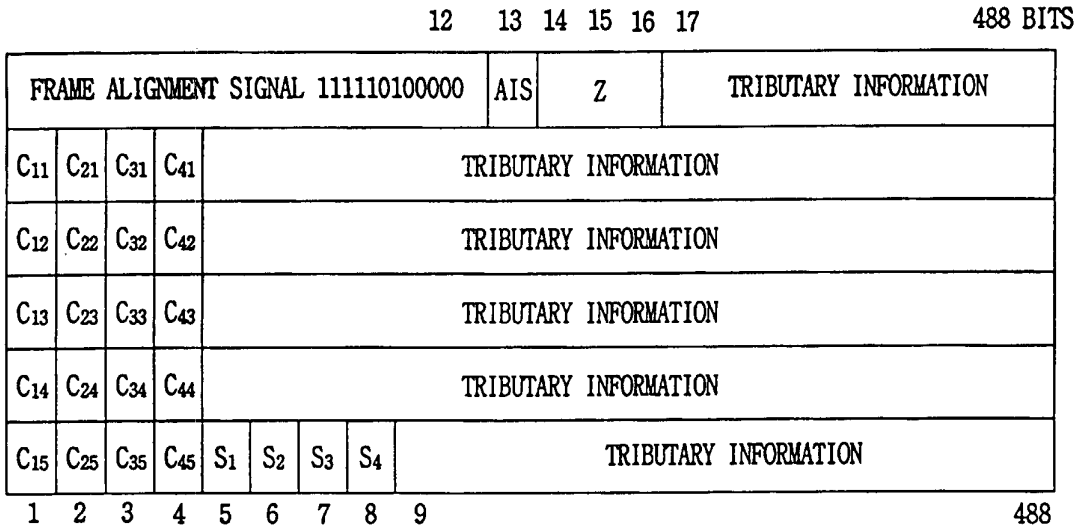

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FIG. 1B

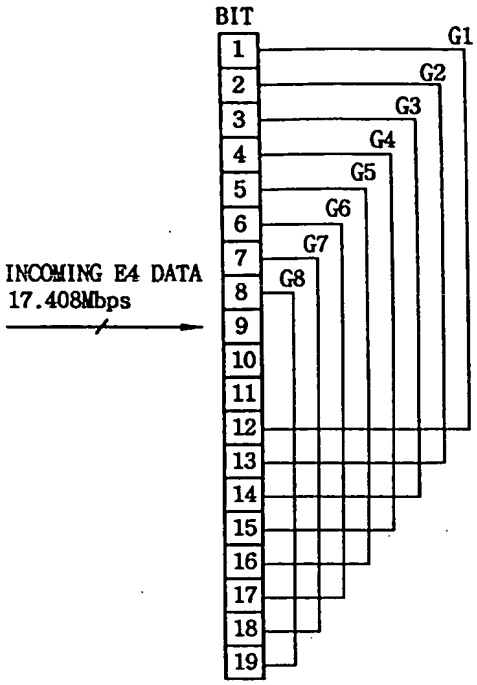

FIG. 1C

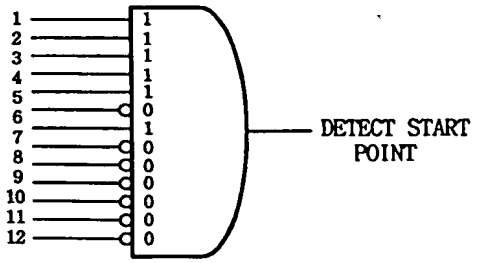

FIG. 1D

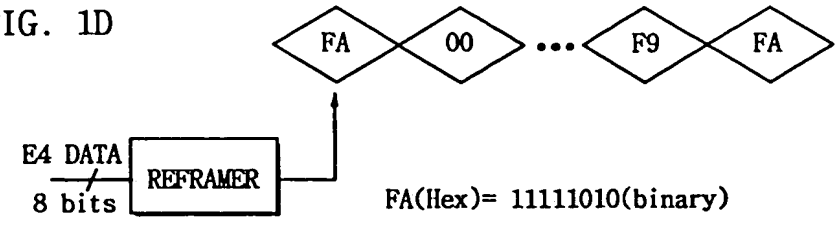

FIG. 2

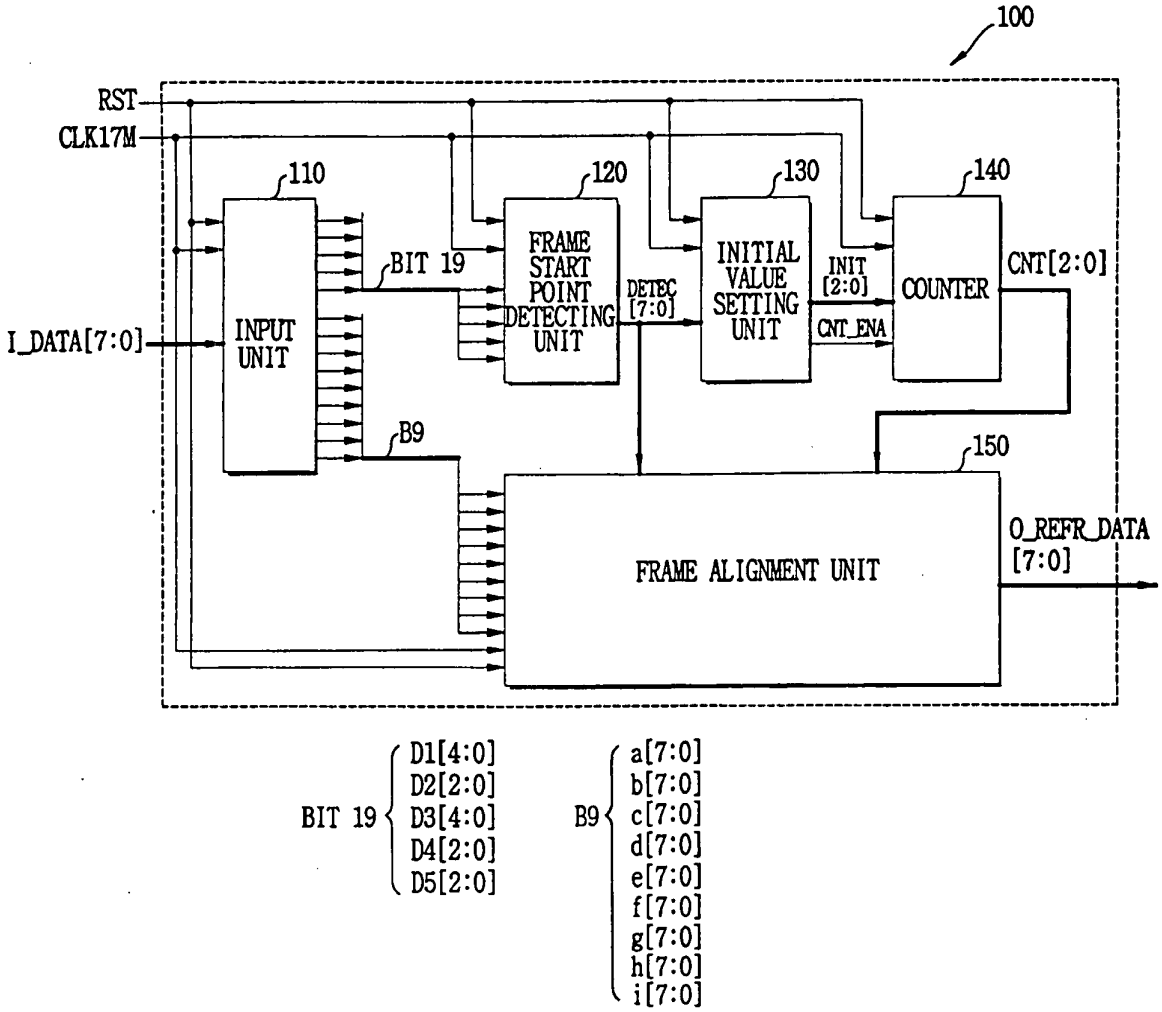

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FIG. 3A

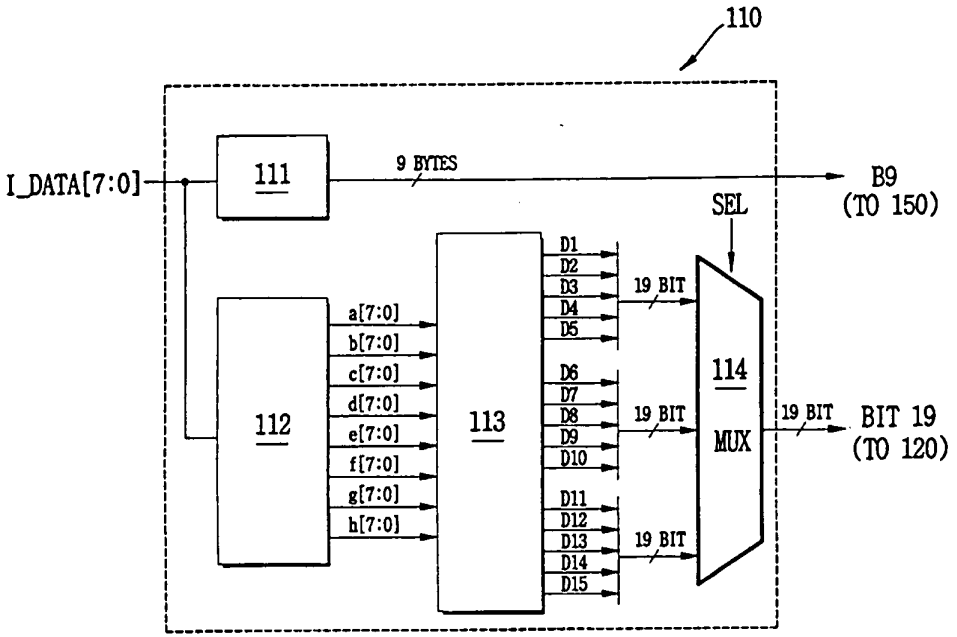

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FIG. 3B

PARALLEL OUTPUT DATA (B9)	1 PERIOD	2 PERIOD	3 PERIOD
a[7:0]	11101100	00101011	10110011
b[7:0]	00110010	·	·
c[7:0]	01010101	·	·
d[7:0]	10101010	·	·
e[7:0]	00001111	·	·
f[7:0]	10100000	·	·
g[7:0]	00000000	·	·
h[7:0]	01100101	·	·
i[7:0]	00101011	10110011	·

FIG. 4

INPUT BIT SEQUENCE	FAS DETECTION	DETEC[7:0]	INIT[2:0]	CNT_ENA	OUTPUT OF COUNTER (140) [2:0]
G1	HIGH	10000000	000	HIGH	000, 001, 010, 011, 100, 101, 110, 111, 000...
G2	HIGH	01000000	001	HIGH	001, 010, 011, 100, 101, 110, 111, 000, 001...
G3	HIGH	00100000	010	HIGH	010, 011, 100, 101, 110, 111, 000, 001, 010...
G4	HIGH	00010000	011	HIGH	011, 100, 101, 110, 111, 000, 001, 010, 011...
G5	HIGH	00001000	100	HIGH	100, 101, 110, 111, 000, 001, 010, 011, 100...
G6	HIGH	00000100	101	HIGH	101, 110, 111, 000, 001, 010, 011, 100, 101...
G7	HIGH	00000010	110	HIGH	110, 111, 000, 001, 010, 011, 100, 101, 110...
G8	HIGH	00000001	111	HIGH	111, 000, 001, 010, 011, 100, 101, 110, 111...

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FIG. 5A

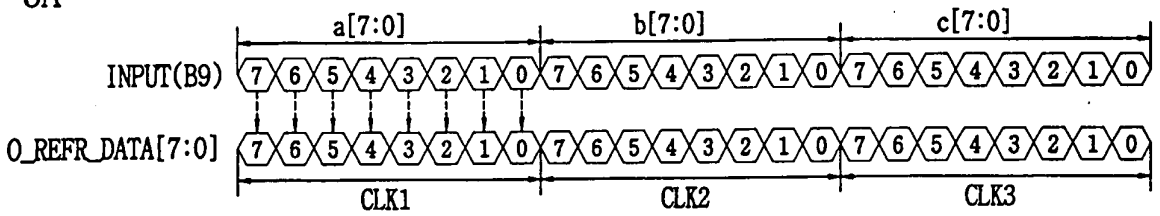


FIG. 5B

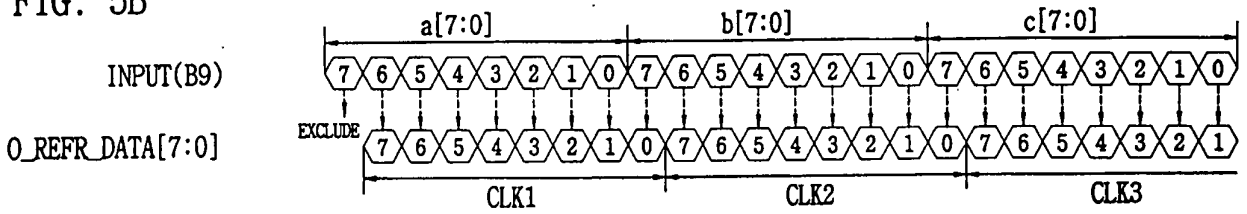
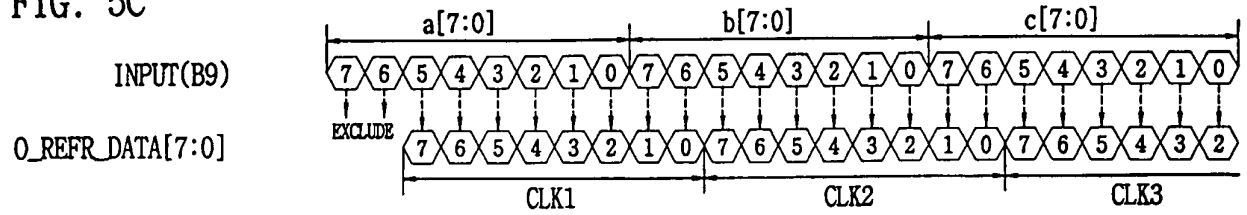


FIG. 5C



09470982.122399

FIG. 5D

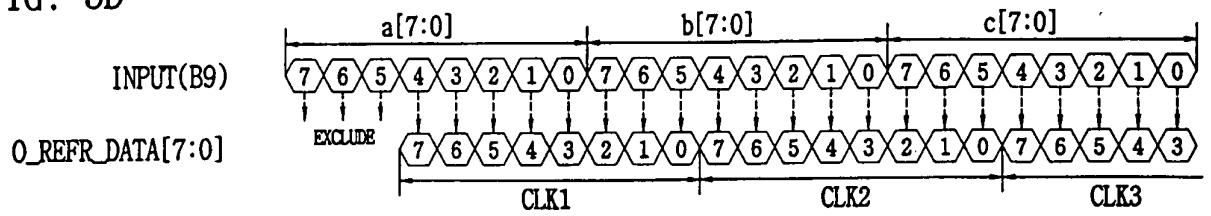


FIG. 5E

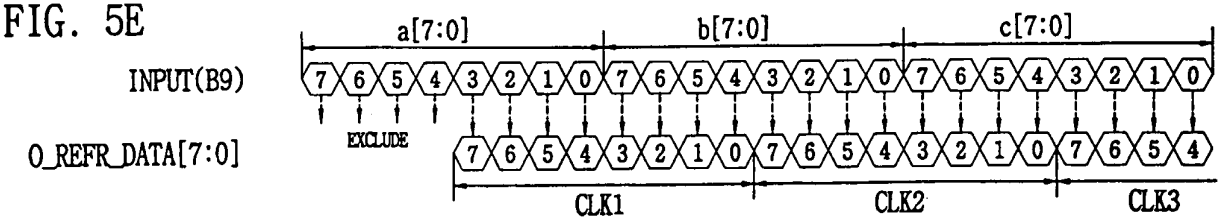


FIG. 5F

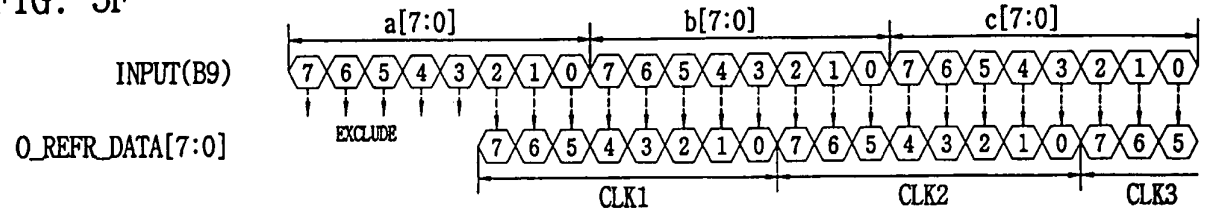


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FIG. 5G

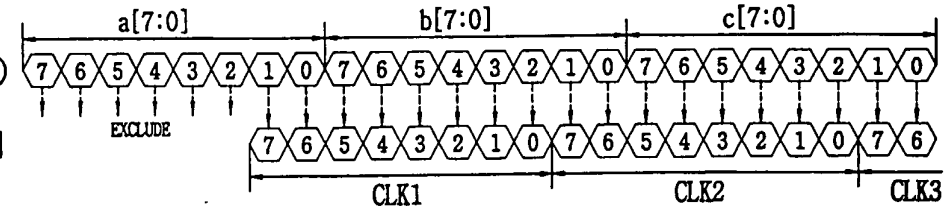
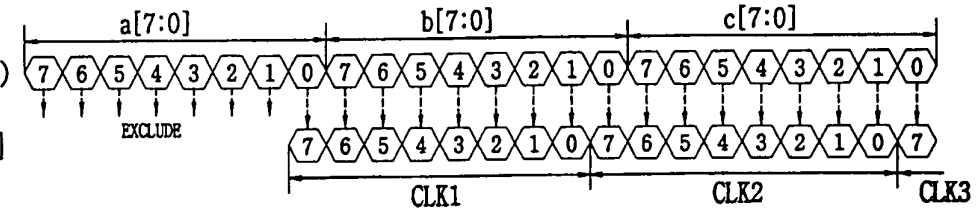
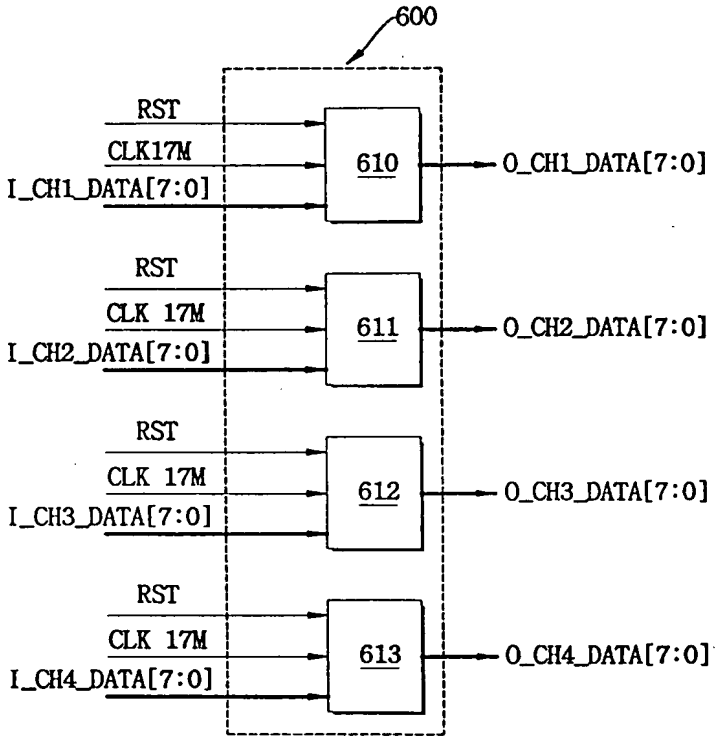


FIG. 5H



09470092.122399

FIG. 6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RST
CLK17M
I_CH1_DATA[7:0]
610
O_CH1_DATA[7:0]
RST
CLK 17M
I_CH2_DATA[7:0]
611
O_CH2_DATA[7:0]
RST
CLK 17M
I_CH3_DATA[7:0]
612
O_CH3_DATA[7:0]
RST
CLK 17M
I_CH4_DATA[7:0]
613
O_CH4_DATA[7:0]

FIG. 7

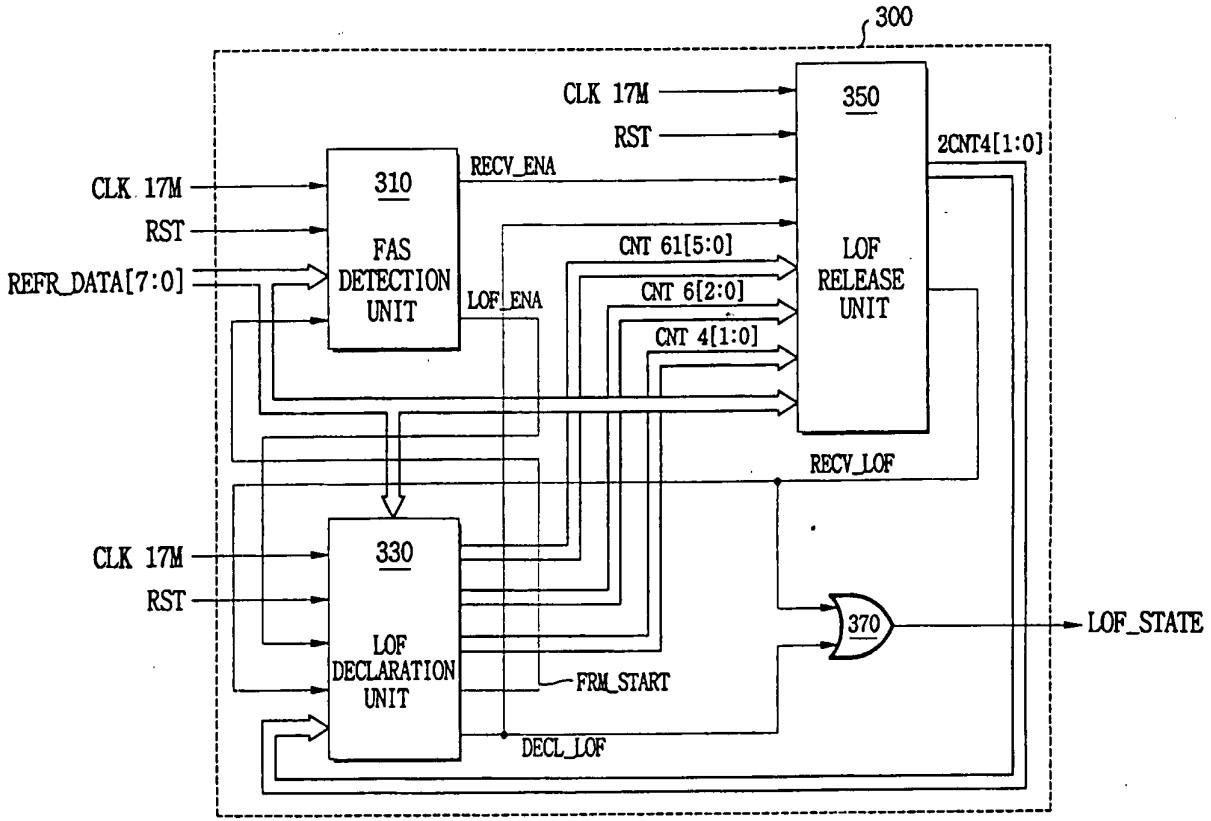

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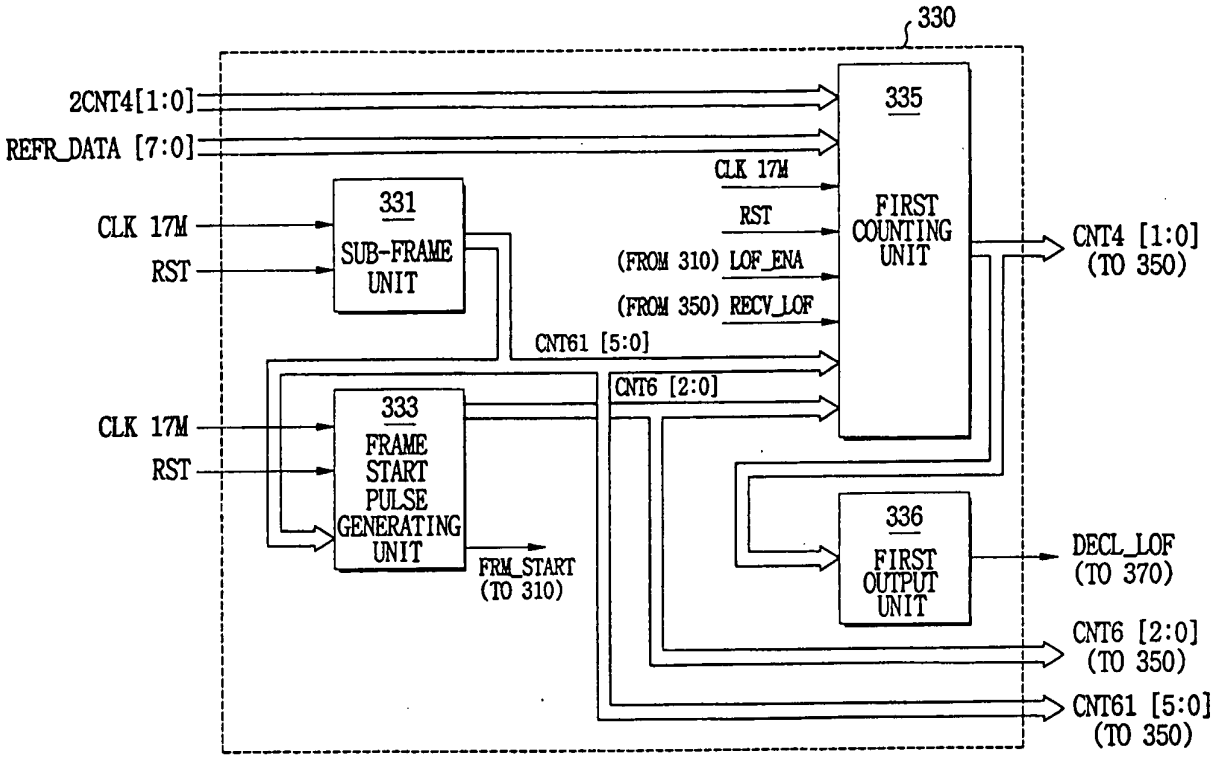
FIG. 8



09470982.122399

FIG. 9

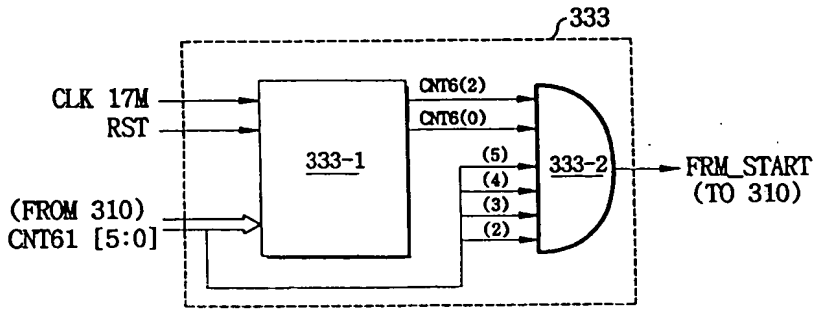


FIG. 10

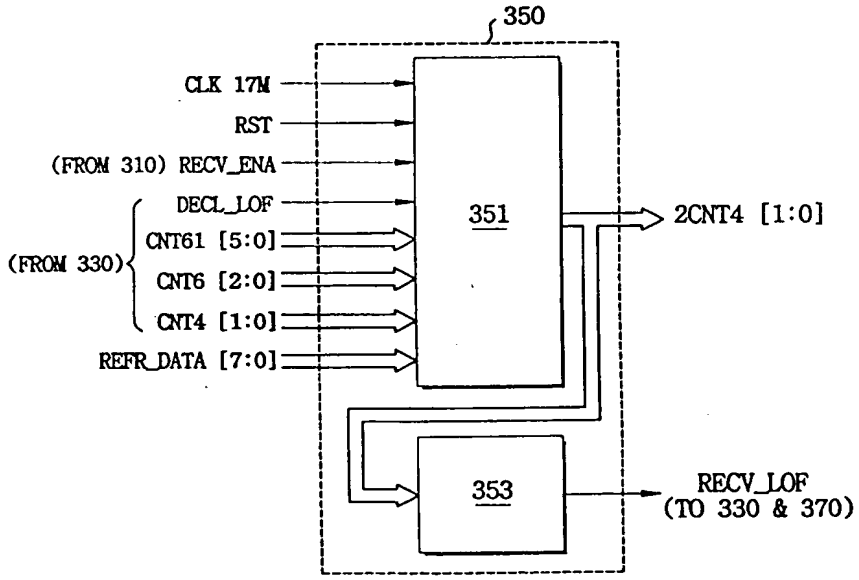
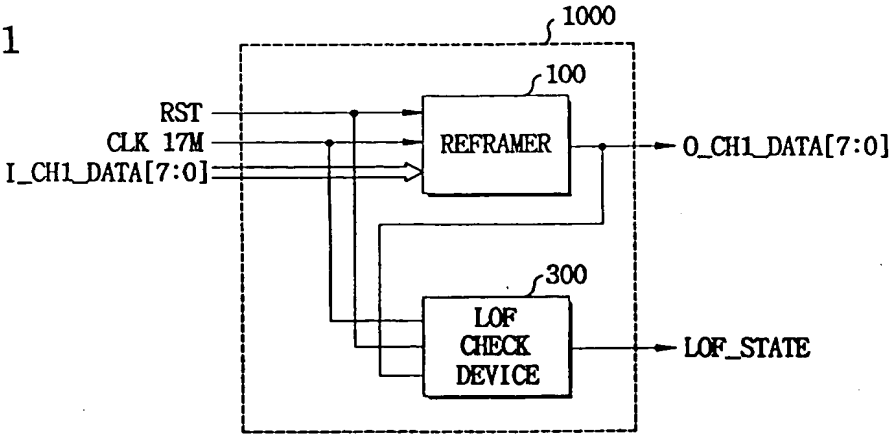


FIG. 11



Sheet 12 of 20

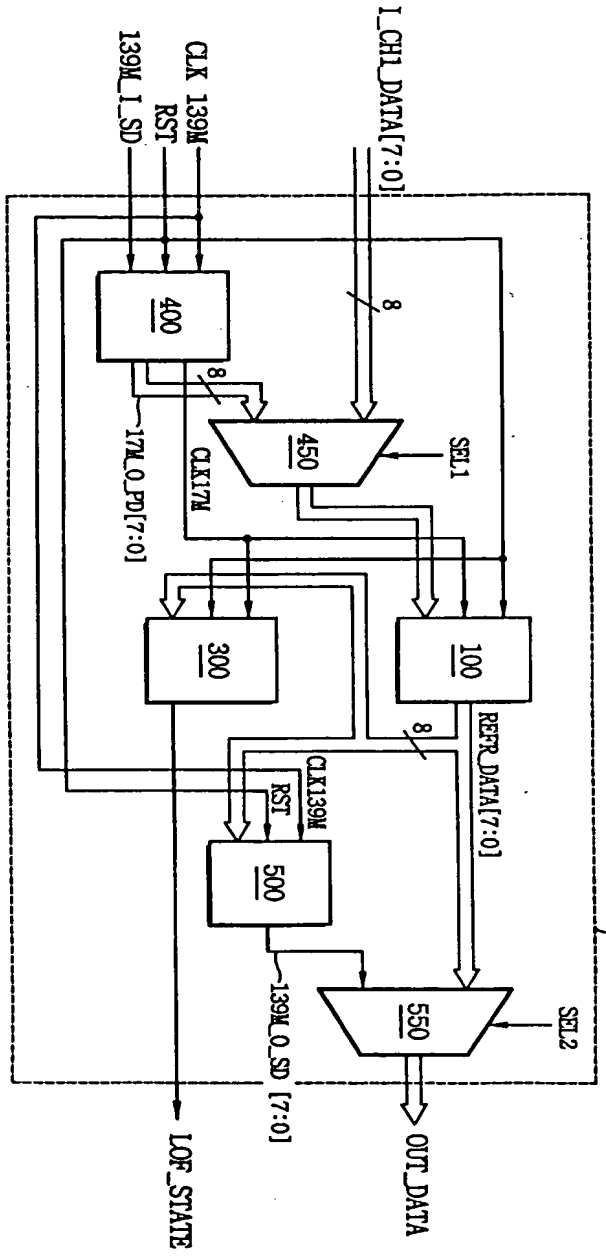
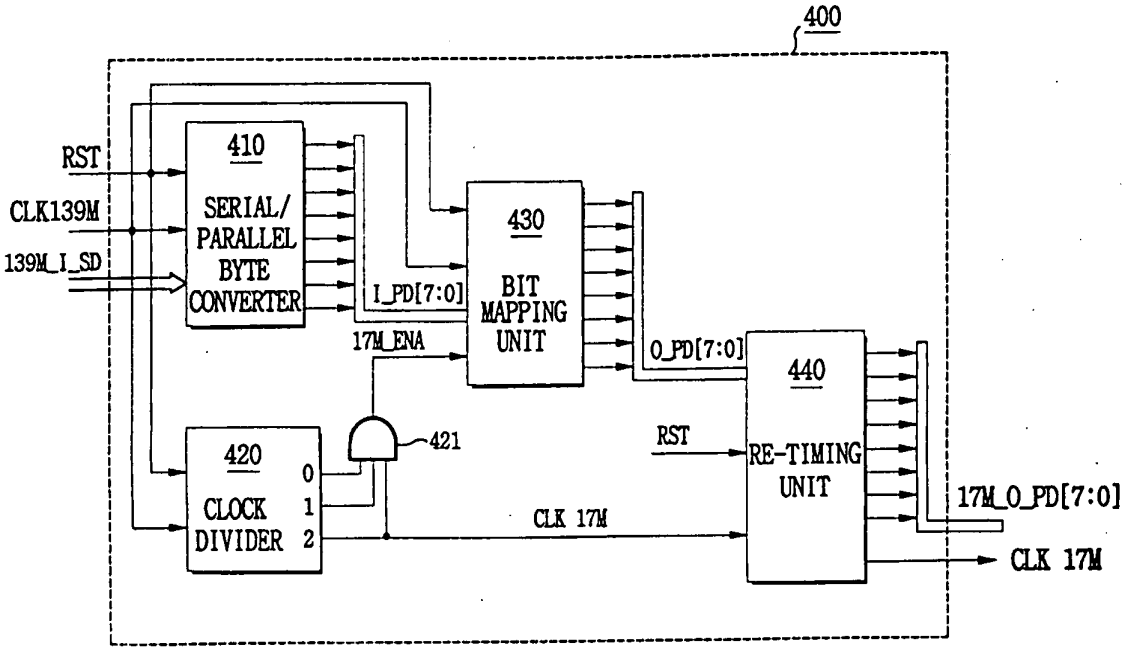


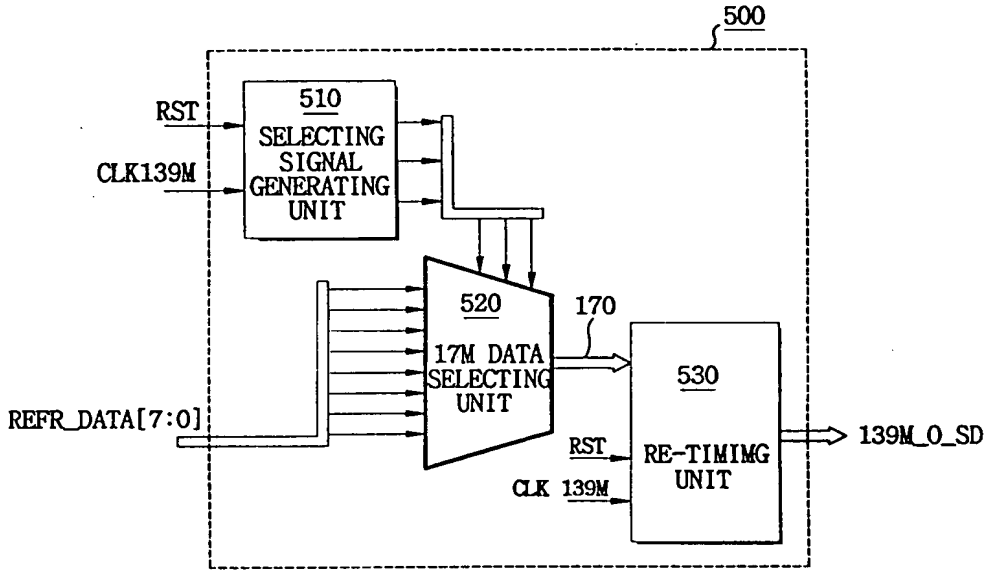
FIG. 12

FIG. 13



0947090A1.123399

FIG. 14


500
510
SELECTING SIGNAL GENERATING UNIT
RST
CLK139M
520
17M DATA SELECTING UNIT
170
530
RE-TIMIMG UNIT
RST
CLK 139M
REFR_DATA[7:0]
139M_O_SD